# 1024-BITS SERIAL ELECTRICALLY ERASABLE PROM

## Features

- State-of-the-art architecture
  - -Non-volatile data storage
  - -Operating voltage Vcc : 2.7-5.5V
  - -Full TTL compatible inputs and outputs
  - -Auto increment read efficient data dump
- Hardware and software write protection
  - -Defaults to write-disabled state at power up
  - -Software instructions for write-enable/disable
  - -Vcc level verification before self-timed programming cycle
- Advanced low voltage CMOS EEPROM technology
- Versatile, easy-to-use interface
  - -Self-timed programming cycle
  - -Automatic erase-bofore-write
  - -Programming status indicator
  - -Word and chip erasable
  - -Stop SK anytime for power savings
- Durability and reliability
  - -40 year data retention
  - -Minimum of 1M write cycles
  - -Unlimited read cycles
  - -ESD protection

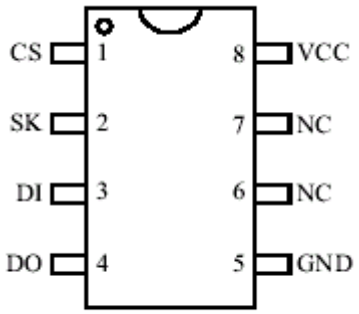
## General Description

The AV93LC46 is a 1024-bit, non-volatile, serial EEPROM. It is manufactured by using advanced CMOS EEPROM technology. The AV93C46 provides efficient non-volatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which includes read,write and write enable/disable functions. The data out pin (DO) indicates the status of the device during the self-timed non-volatile programming cycle.

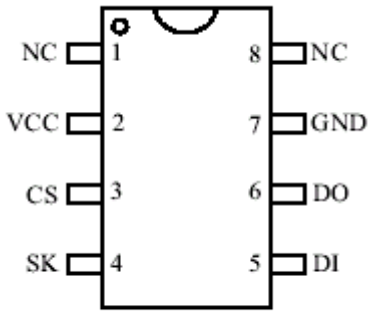
The self-timed write cycle includes an automatic erase-before write capability. Only when the chip is in the WRITE ENABLE state and proper Vcc operation range is the WRITE instruction accepted and thus to protect Against inadvertent writes, Data is written in 16 bits per write instruction into the selected register. If chip select (CS) is brought HIGH after initiation of the write cycle, the data output (DO) pin will indicate the READY/BUSY status of the chip.

The AV93C46 is available in space-saving 8-lead PDIP, 8-lead SOP and rotated 8-lead SOP package.

## CONNECTION DIAGRAM




PDIP-8L / SOP-8L




Rotated SOP-8L

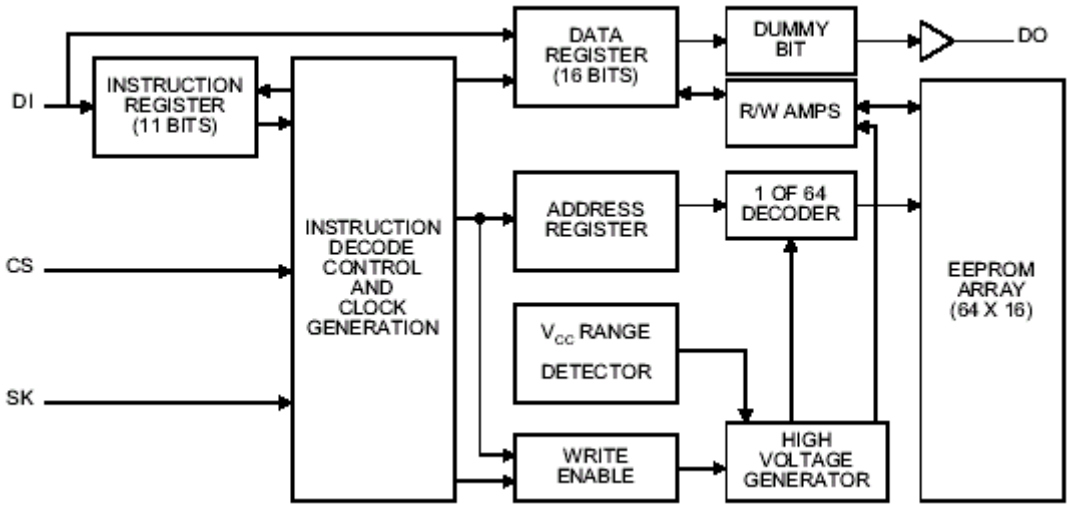
## PIN ASSIGNMENT

| | |
|---|---|
| CS | Chip Select |
| SK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| GND | Ground |
| VCC | Power Supply |
| NC | No Connection |

## ORDERING INFORMATION

AV93LC46 XX
AV ----------AVIC Electronics CO.,LTD
LC ----------Operating Voltage : 2.7~5.5V, CMOS
46 ----------Type : 1K
XX --------- SC/PC/SI/PI/TC/TI
(**S**----SOP8; **P**----DIP8; **T**----TSSOP; **C**----0℃~+70℃; **I**---- -45℃~+80℃)

## Block Diagram




## Absolute Maximum Ratings

Storage Temperature……. –65℃ to +125℃
Voltage with Respect to Ground……-0.3 to +6.5 V
NOTE:These are STRESS rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

## Operating Conditions

Temperature under bias AV93LC46……0℃ to +70℃

## DC Electrical Characteristics (Vcc=2.7V-5.5V,Ta=25℃, unless otherwise noted)

| symbol | Parameter | conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Icc1 | Operating Current (Program) | SCL=10KHz CMOS Input Leavels | - | 3 | mA |
| Icc2 | Operating Current (Read) | SCL=10KHz CMOS Input Leavels | - | 200 | uA |
| $I_{SB1}$ | Stabdby Current | SCL=SDA=0V,Vcc=5V | - | 10 | uA |
| $I_{SB2}$ | Stabdby Current | SCL=SDA=0V,Vcc=3V | - | 1 | uA |
| $I_{IL}$ | Input Leakage | $V_{IN}$=0V to Vcc | -1 | +1 | uA |
| $I_{OL}$ | Output Leakage | Vout=0V to Vcc | -1 | +1 | uA |
| $V_{IL}$ | Input Low Voltage** | | -0.1 | Vcc X 0.3 | V |
| $V_{IH}$ | Input High Voltage** | | Vcc X 0.7 | Vcc+0.2 | V |
| $V_{OL1}$ | Output Low Voltage | $I_{OL}$=2.1mA TTL | - | 0.4 | V |
| $V_{OL2}$ | Output Low Voltage | $I_{OL}$=10uA CMOS | - | 0.2 | V |
| $V_{LK}$ | Vcc Lockout Voltage | Programming Command Can Be Executed | Default | - | V |

Note. ** $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested

## AC Electrical Characteristics (Vcc=2.7V – 5.5V, Ta=25℃ unless otherwise noted )

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $F_{SK}$ | SK Clock Frequency | | 0 | 1 | MHz |
| $T_{SKH}$ | SK High Time | | 250 | | ns |
| $T_{SKL}$ | SK Low Time | | 250 | | ns |
| $T_{CS}$ | Minimum CS Low Time | | 250 | | ns |
| $T_{CSS}$ | CS Setup Time | Relative to SK | 50 | | ns |
| $T_{DIS}$ | DI Setup Time | Relative to SK | 100 | | ns |
| $T_{CSH}$ | CS Hold Time | Relative to SK | 0 | | ns |
| $T_{DIH}$ | DI Hold Time | Relative to SK | 100 | | ns |
| $T_{PD1}$ | Output Delay to “1” | AC Test | | 500 | ns |
| $T_{PD0}$ | Output Delay to “0” | AC Test | | 500 | ns |
| $T_{SV}$ | CS to Status Valid | AC Test CL=100pF | | 500 | ns |
| $T_{DF}$ | CS to DO in 3-state | CS=VIL | | 100 | ns |
| $T_{WP}$ | Write Cycle Time | | | 10 | ms |
| Endurance** | 5V,25℃,Page Mode | | 1M | | Write cycles |

Note. ** The Parameter is characterized and isn’t 100% tested.

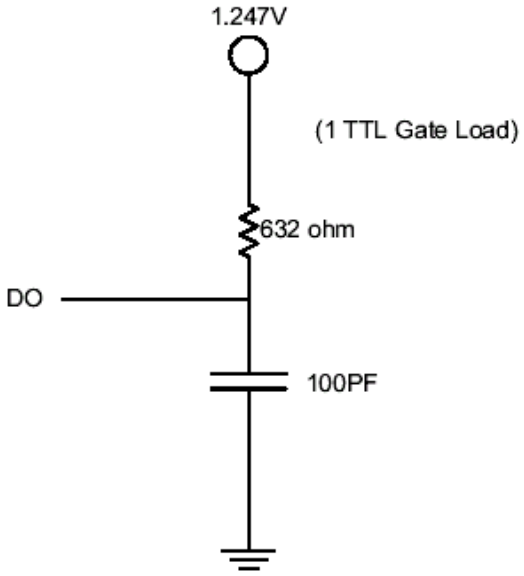



FIGURE 1. AC TEST CONDITIONS

## Instruction Set

| Instruction | Start Bit | OP Code | Address | Input Data |
|---|---|---|---|---|
| READ | 1 | 10 | A5-A0 | |
| WEN(Write Enable) | 1 | 00 | 11XXXX | |
| WRITE | 1 | 01 | A5-A0 | D15-D0* |
| WRALL (Write all Registers) | 1 | 00 | 01XXXX | D15-D0* |
| WDS (Write Disable) | 1 | 00 | 00XXXX | |
| ERASE | 1 | 11 | A5-A0 | |
| ERAL (Erase All Registers) | 1 | 00 | 10XXXX | |

* If input Data is not 16 bits exactly, the last 16 bits will be taken as input data ( a word )

## Pin Capacitance ** (Ta=25℃, f=1MHz)

| Symbol | Parameter | Max | Units |
|---|---|---|---|
| Cout | Output Capacitance | 5 | pF |
| $C_{IN}$ | Input Capacitance | 5 | pF |

Note. ** The Parameter is Characterized and isn't 100% tested.

## Functional Descriptions

**Applications**
The AV93LC46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Typical applications include robotics, alarm devices, electronic locks, meters and instrumentation settings such as LAN cards, monitors and MODEM.

**Endurance and Data Retention**
The AV93LC46 is designed for applications requiring up to 1000K programming cycles (WRITE, WRALL, EARSE and ERAll). It provides 40 years of secure data retention without power after the execution of 1000K programming cycles.

**Device Operation**
The AV93LC46 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin.
Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the AV93LC46 will remain in its last state. This allows full static flexibility and maximum power conservation.

**Read (READ)**
The READ instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) the output on DO changes during the rising edge transitions of SK. (Shown in Figure 3 )

**Auto Increment Read Operations**
Sequential read is possible, since the AV93LC46 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations (the address "0000" is assumed as the higher address of "111111") is output. The address will wrap around continuously with CS high until the chip select (CS) control pin is brought low. This allows for single instruction data dumps to executed with a minimum of firmware overhead.

**Write Enable (WEN)**
Before any device programming (WRITE, WRAll, ERASE, and ERAl) can be done, the WRITE ENABLE (WEN) instruction must be executed first. When Vcc is applied, this device powers up in the WRITE DISABLE state. The device then remains in a WRITE DISABle state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until Vcc is removed. (NOTE: Neither the Wen nor the WDS instruction has any effect on the READ instruction.) (Shown in Figure 4.)

**Write Disable (WDS)**
The WRITE DISABLE (WDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the WRITE DISABLE state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (Shown in Figure 5.)

## Functional Description (Continued)

**Write (WRITE)**
The WRITE instruction includes 16 bits of data to be written into the specified register . After the last bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the selftimed programming cycle.

After a minimum wait of 250ns (5V operation) from the falling edge of CS (tcs), DO will indicate the READY/BUSY status of the chip if CS is brought HIGH. This means that logical "0" implies the programming is still in progress while logical "1" indicates the selected register has been written, and the part is ready for another instruction.(See Figure 6.)

**Note:** The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag,not to reset it through this combination of control signals.

Before a WRITE instruction can be executed, the device must be in the WRITE ENABLE (WEN) state.

**Write All (WRALL)**
The write All (WRALL) instruction programs all registers with the data pattern specified in the instruction. While the WRALL instruction is being loaded, the address field becomes a sequence of DON'T-CARE bits. (Shown in Figure 7.)

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of of 250ns (tcs), the DO pin indicates the READY/BUSY status of the chip. (Shown Figure 7.)

**ERASE (ERASE)**
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after minimum of tcs, will cause DO to indicate the READY/BUSY status of the chip. To explain this, a logical "0" indicates the programming is still in progress while a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (Shown in Figure 8.)

**Erase All (ERALL)**
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all the entire memory array a logical "1". (Shown in Figure 9.)

**Security Consideration**
To protect the entire part against accidental modification of data, each programming instruction (WRITE, WRALL, ERASE, and ERALL) must satisfy two conditions before user initiate self-timed programming cycle (the falling edge of CS). One is that the AV93LC46 is at WEN status. The other is that Vcc value must exceed a lock-out value which can be adjusted by AVIC.

## Timing Diagram (1)

**Organization Key**

| I/O | AV93LC46 (1K) | | AV93LC56 (2K) | |
|---|---|---|---|---|
| | X 8 | X 16 | X 8 | X 16 |
| AN | A6 | A5 | A8(1) | A7(2) |
| DN | D7 | D15 | D7 | D15 |

Note : (1). A8 is a DON'T CARE value, but the extra clock is required.
(2). A7 is a DON'T CARE value, but the extra clock is required.

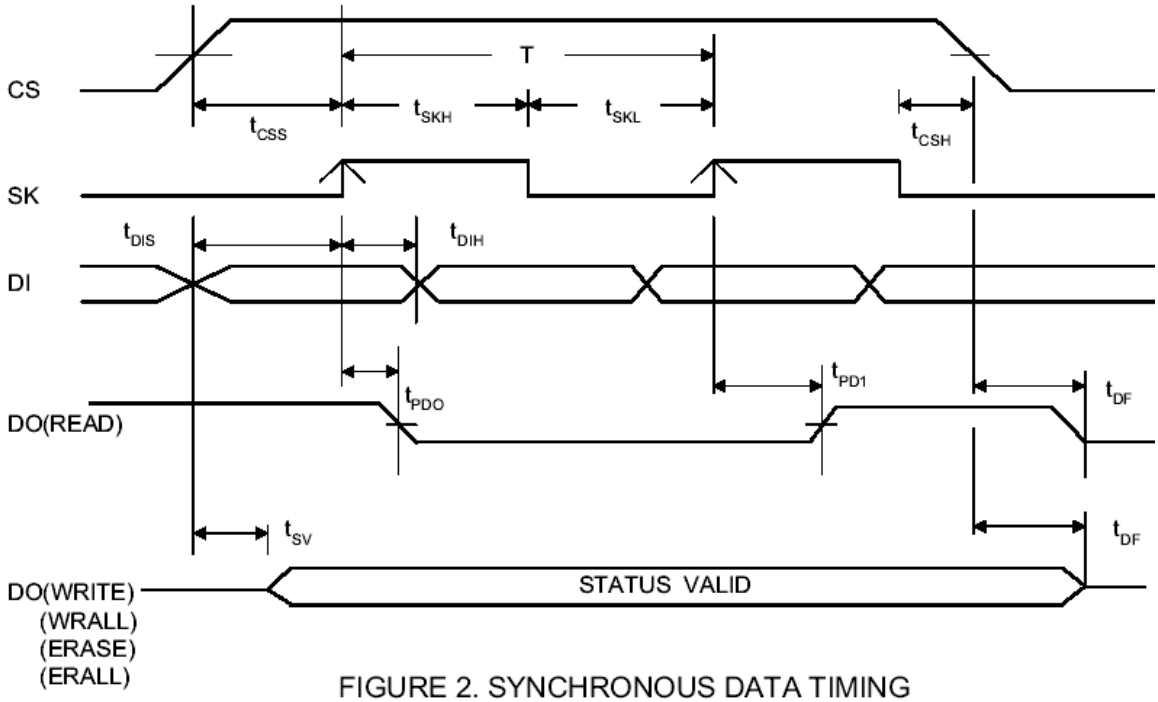
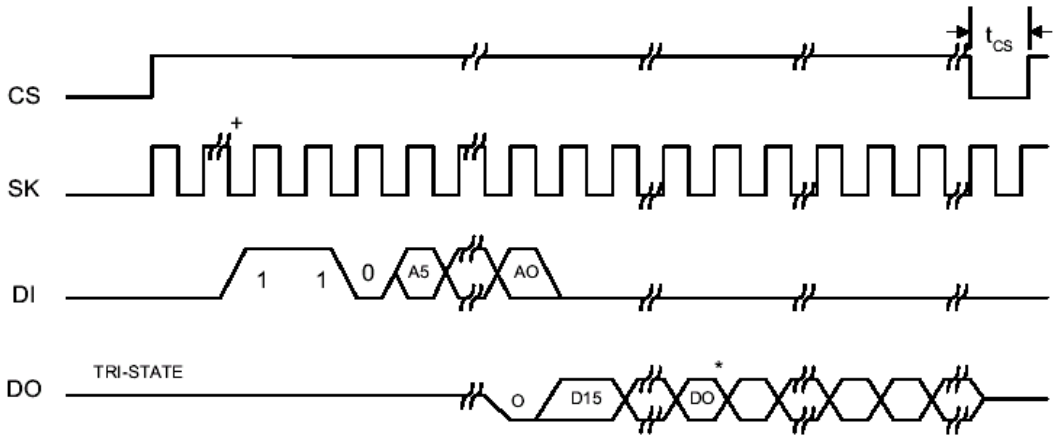


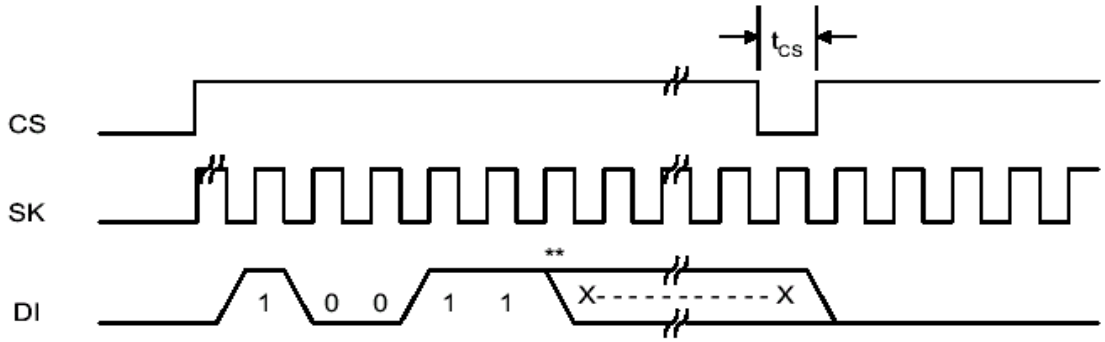

FIGURE 2. SYNCHRONOUS DATA TIMING




+For all instructions, SK cycles before start bit don't care.
*Address Pointer Cycle to the Next Register.

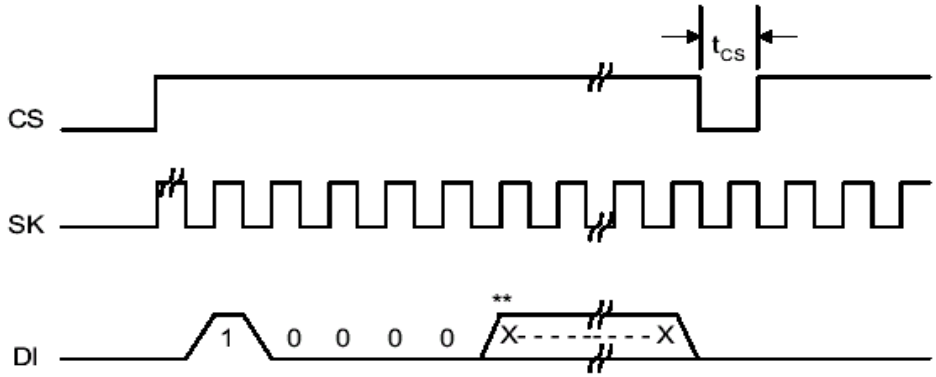
FIGURE 3. DATA READ CYCLE TIMING

## Timing Diagram (2)




DO = TRI-STATE
**A3~A0 don't care.

FIGURE 4. WRITE ENABLE(WEN) CYCLE TIMING




DO = TRI-STATE
**A3~A0 don't care.

FIGURE 5. WRITE DISABLE(WDS) CYCLE TIMING

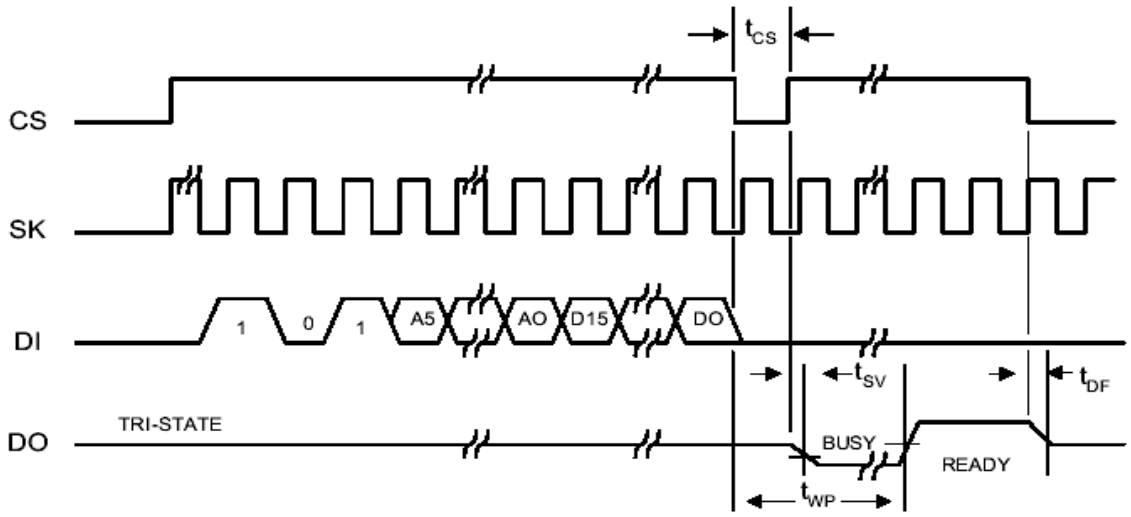



FIGURE 6. WRITE(WRITE) CYCLE TIMING

## Timing Diagram (3)

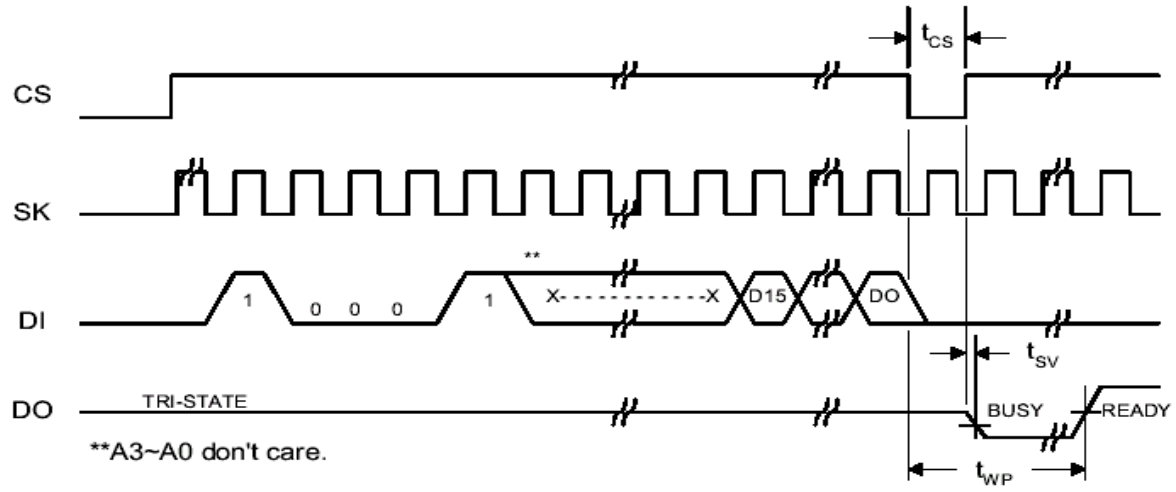



FIGURE 7. WRITE ALL(WRALL) CYCLE TIMING

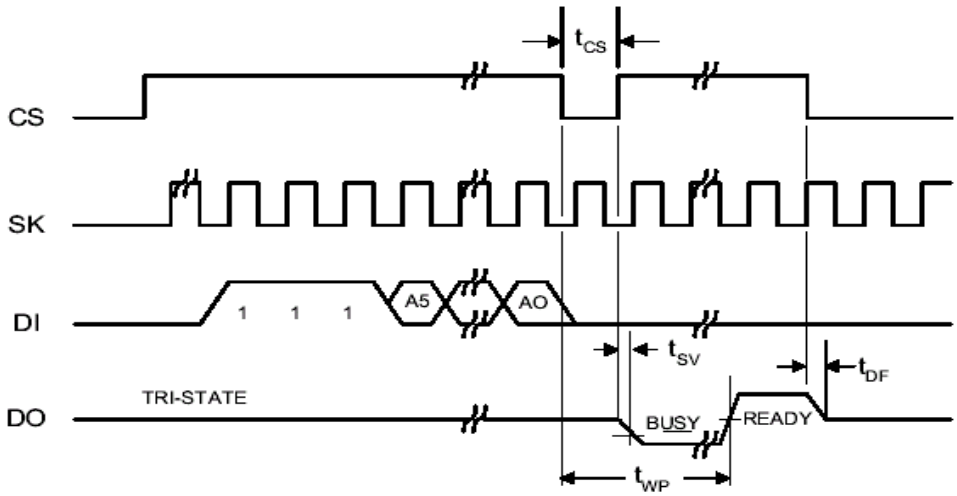



FIGURE 8. ERASE(ERASE) CYCLE TIMING

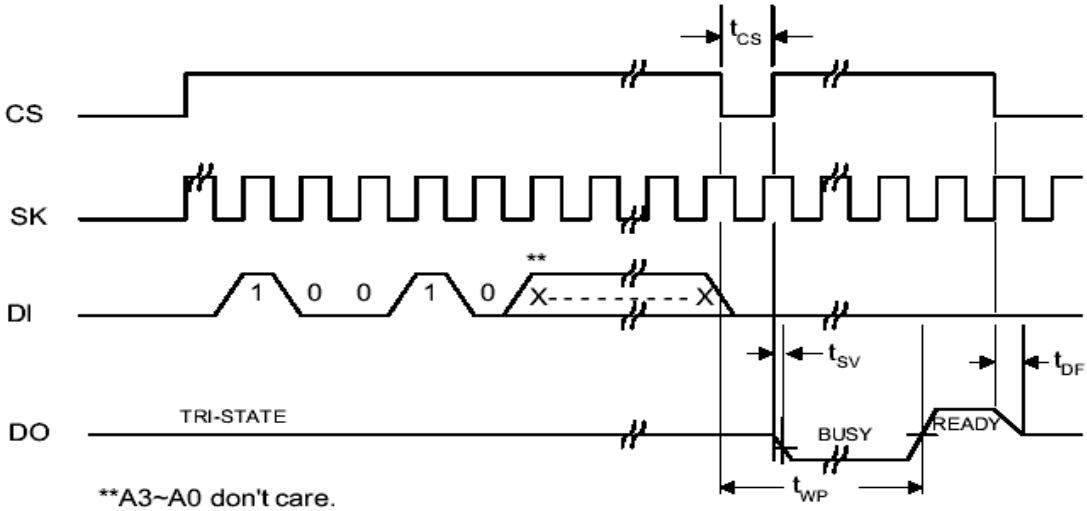



FIGURE 9. ERASE ALL(ERALL) CYCLE TIMING